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tegrated circuit such as a RAM in which grooves are formed in a semiconductor body. The side walls of the groove are covered by an insulating film. The interior of the groove is filled by conductive material forming a first electrode of a capacitor, the other electrode is formed by a doped layer surrounding the groove, and having a conductivity type opposite to that of the substrate.

Summary of the Invention

The object of the present invention is to provide a semiconductor memory which has a capacitor with good characteristics but requires only a small space, yet overcoming the serious problems such as the alpha-particle induced disturbances that arise with a decrease in size of a memory cell, while maintaining high S/N ratio and breakdown voltage.

These objects are achieved by the features of claim 1.

Brief Description of the Drawing

The single Figure is a section view through an embodiment of the present invention.

Detailed Description of the Invention

In the embodiment described below, a memory is provided which has a capacitor in a memory capacitor portion which has an increased capacity without requiring an increase space, and which is hardly affected at all by external noise, the capacitor being constructed within a groove formed in the substrate.

In the drawing, reference numeral 3 denotes a bit line, 4 a word line, 10 a p-type silicon substrate. 12 a first intermediate insulation film, 14 a second intermediate insulation film, 15 an n-type diffusion layer, 17 a groove, 18 a capacitor insulation film, 19 a capacitor electrode, 23 an SOI layer, and 24 a transistor channel.

For forming this embodiment, a groove 17 is etched in the substrate 10, thereafter the capacitor insulation film 18 is desposited in the groove and then a single crystalline silicon film is formed on said insulation film 18, thereby forming an SOI (silicon-on-insulator) construction which includes places that will become the capacitor electrode 19 and the diffusion layer 15 in subsequent steps. Namely, a polycrystalline or amorphous silicon film is deposited over the whole surface, or over part of the surface , and the whole or part of the surface is heated by a laser beam or by a heater, so that a monocrystalline layer 23 grows on the insulation film after the silicon film melts, or with the silicon film maintained in the solid phase. Although not shown, the monocrystallization takes place easily if a piece of silicon film of SOI construction is brought into contact with the silicon substrate 10.

Thereafter, a gate oxide film 12 and a gate 4 are deposited on the SOI layer 23, followed by the formation of an n^+-type layer, so that one side acts as the capacitor electrode 19 and the other side as the diffusion layer 15 connected to the bit line 3. No switching transistor 2 is formed in the silicon substrate 10; i.e., the substrate 10 may be of any conductivity type. That is, if the substrate 10 is n-type, the silicon substrate 10 itself acts as a plate.

A dynamic memory, in general, has peripheral circuits with various functions formed around the memory cell, and it is difficult to make the whole of the silicon substrate 10 n-type. In this case, however, a doped layer may be provided as a plate, and only the portion of the memory cell need be n-type.

In this embodiment the groove has a simple rectangular shape, as shown in Fig. 1. Capacity increases with an increase in the surface area of the capacitor electrode 19. Therefore, the capacitor can be increased to more than that of a simple rectangular shape, while maintaining the same space. That is, the capacity can be increased by forming the groove in a comb shape or in two or more small grooves or in an annular groove. Therefore, individual steps can be replaced by others in a variety of ways. In all the embodiments, however, the common point remains that the side walls of the groove formed in the substrate are utilized as a capacitor part.

The word line 4 has the form of a continuous gate within a memory cell array. It is, however, also possible to form polycrystalline silicon transfer gates of switching transistors that are not continuous, but are separate between memory cells, and connect the gates by the word line 4 using new contact holes. This makes it possible to achieve a high switching speed by using polycrystalline silicon gates which have heretofore been evaluated for their reliability, and by utilizing the advantage of the low resistance of aluminum.

In the embodiment shown in the drawing, a transistor channel is 24 is formed in the vertical in the vertical direction within the SOI layer 23. The vertical junction transistor can be adapted to every kind of memory cell which employs SOI.

As described in the beginning, the invention deals with the use of an n-channel MOS transistor. To form a p-channel transistor, impurities of the opposite conductivity type should be used. Namely, the phosphorus or arsenic ions should be replaced with boron or aluminum ions, and the boron

(18) und eine in der Nut (17) auf der Isolierschicht (18) ausgebildete zweite Elektrode (19) umfaßt und mit Source oder Drain des Feldeffekttransistors gekoppelt ist,

dadurch gekennzeichnet, daß der Feldeffekttransistor über dem Kondensator ausgebildet ist und der Kanal (24) des Feldeffekttransistors vertikal verläuft.

2. Halbleiterspeicher nach Anspruch 1, wobei der Kanal (24) des Feldeffekttransistors innerhalb einer einkristallinen Schicht (23) ausgebildet ist.

3. Halbleiterspeicher nach Anspruch 1 oder 2, wobei die Gate-Isolierschicht (12) des Feldeffekttransistors und die Isolierschicht (18) des Kondensators in unterschiedlichen Schritten ausgebildet sind.

4. Halbleiterspeicher nach einem der Ansprüche 1 bis 3, wobei die Source- oder die Drain-Zone (15) des Feldeffekttransistors in einer Querschnittsebene zu beiden Seiten von dessen Gate-Elektrode (4) vorgesehen ist.

5. Halbleiterspeicher nach einem der Ansprüche 1 bis 4, wobei die Gate-Elektrode (4) des Feldeffekttransistors in einer Vertiefung ausgebildet ist.

6. Halbleiterspeicher nach Anspruch 5, wobei der Kanal (24) des Feldeffekttransistors an einer Seitenwand der Vertiefung vorgesehen ist.